IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket No. 13158US02

In the Application of:

Craig Hemsing

U.S. Serial No.:	10/003,563
Filed:	October 24, 2001
For:	NETWORK TELEPHONY DEVICE
Examiner:	Nasser G. Moazzami
Group Art Unit:	2187
Conf. No.:	5055

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop: Appeal Brief-Patents, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on January 17, 2006.

John A. Wiberg
Reg. No. 44,401

BRIEF ON APPEAL

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from an Office Action dated March 15, 2005, in which claims 1-26 were finally rejected.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California, and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment recorded at Reel 012634, Frame 0456 in the PTO assignment search room.

RELATED APPEALS AND INTERFERENCES

There currently are no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-25 are pending in the present application. Claim 26 is cancelled in an amendment submitted herewith. Pending claims 1-25 stand rejected and are the subject of this appeal.

STATUS OF THE AMENDMENTS

An amendment is submitted herewith to cancel claim 26. Because this amendment merely cancels a claim, Appellant submits that it complies with 37 C.F.R. 1.116 and should be entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to an apparatus for reducing the memory footprint of a first processor device. The apparatus includes a segment of program code which is split into portions including at least one controlling piece and at least one separate working piece. A storage area is operable to store certain pieces of the program code. A first memory area associated with the first processor device is operable to receive certain portions of the program code. A hardware transfer mechanism efficiently links the storage area with the first memory area. The memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and transferring only certain working pieces of the program code in the first memory area.

The invention of claim 1 is illustratively described in the Specification of the present application at, for example, paragraphs 53 and 54, referring to Figure 4. FIG. 4 shows a first processor device 402. A segment of program code is split into a controlling piece 406 and working piece(s) 404. The working piece(s) 404 of the program code is stored in a memory area of the first processor device 402. The controlling piece 406 of the program code is stored in a storage area of a second processor device 408, thereby reducing the memory footprint of the first processor. A hardware transfer mechanism 410 efficiently links the storage area of second processor device 408 with the memory area of the first processor device 402. The invention of claim 1 is also described in other parts of the application, such as in the Summary of the Invention section.

Claims 2-12 are dependent upon claim 5.

Claim 13 is directed to an method for reducing the memory footprint of a first processor device. Pursuant to the method, a segment of program code is split into portions including at least one controlling piece and at least one separate working piece. Certain portions of the program code are stored in a storage area. Certain portions of the program code are received in a first memory area associated with the first processor device. The storage area is linked with the first memory area using an efficient hardware transfer mechanism. The memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and only certain working pieces of the program code in the first memory area.

The invention of claim 13 is illustratively described in the Specification of the present application at, for example, paragraphs 53 and 54, referring to Figure 4. FIG. 4 shows a first processor device 402. A segment of program code is split into a controlling piece 406 and working piece(s) 404. The working piece(s) 404 of the program code is stored in a memory area of the first processor device 402. The controlling piece 406 of the program code is stored in a storage area of a second processor device 408, thereby reducing the memory footprint of the first processor. A hardware transfer mechanism 410 efficiently links the storage area of second processor device 408 with the memory area of the first processor device 402. The invention of claim 13 is also described in other parts of the application, such as in the Summary of the Invention section.

Claims 14-24 are dependent upon claim 13.

Claim 25 is directed to a distributed signal processing framework for reducing the memory footprint of a digital signal processing device. The framework includes a signal processing algorithm, a low-MIPS processor device, a high-MIPS processor device and a hardware transfer mechanism. The signal processing algorithm is split into a controlling piece and at least one separate processing piece. The low-MIPS processor device has a high-memory footprint. The controlling piece is stored and runs on the low-MIPS processor device. The high-MIPS processor has a low-memory footprint. At least one of the separate processing pieces is stored and runs on the high-MIPS processor device. The hardware transfer mechanism efficiently links the pieces through the distributed framework.

The invention of claim 25 is illustratively described in the Specification of the present application at, for example, paragraphs 52-54, referring to Figure 4. FIG. 4 shows a first processor device 402. A segment of program code is split into a controlling piece 406 and working piece(s) 404. The working piece(s) 404 of the program code is stored in a memory area of the first processor device 402. The controlling piece 406 of the program code is stored in a storage area of a second processor device 408. A hardware transfer mechanism 410 efficiently links the pieces 404 and 406. Paragraph 52 says, "The first processing device would include a DSP (or similar memory constrained device), and the second processing device would include a MCU (or similar processor with lower-cost memory)." Paragraph 52 also says that "the preferred method of distributing the processing includes locating the low-MIPS, high-memory footprint part of the algorithm (i.e., the controlling piece) on the MCU device block. The high-MIPS, lower-memory footprint part of the algorithm (i.e., the working piece) remains on the DSP device block. The invention of claim 25 is also described in other parts of the application, such as in the Summary of the Invention section.

GROUNDS OF REJECTION TO BE REVIWED ON APPEAL

I. Claims 1-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,175,830 issued to Arthur M. Sherman, et al.

ARGUMENT

I. Claims 1-25 are not anticipated under 35 U.S.C. § 102(b) by Sherman et al. (US 5,175,830).

In the Office Action of March 15, 2005, the Examiner rejected claims 1-25 under 35 U.S.C. § 102(b) as being anticipated by Nagano (US 5,175,830). 35 U.S.C. 102(b) states:

> A person shall be entitled to a patent unless... the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.[1]

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[2]

A. Claims 1-24 are not anticipated under 35 U.S.C. § 102(b) by Sherman et al. (US 5,175,830).

Claim 1 is directed to

> 1. An apparatus for reducing the memory footprint of a first processor device, the apparatus comprising:
> a segment of program code which is split into portions including at least one controlling piece and at least one separate working piece;
> a storage area for storing certain pieces of the program code;
> a first memory area associated with the first processor device for receiving certain portions of the program code; and
> a hardware transfer mechanism for efficiently linking the storage area with the first memory area,
> wherein the memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and transferring only certain working pieces of the program code in the first memory area.

The Examiner asserted that claim 1 is disclosed in Sherman, column 1, lines 65-67; column 2, lines 6-27; and column 3, lines 38-60. Appellant respectfully submits that

[1] 35 U.S.C. 102(b)

[2] *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Sherman involves "differentiating the overlays into a *code portion* and into a *data portion*"[3] (emphasis added). Claim 1, in contrast, refers to "a segment of program code which is split into at least one *controlling piece* and at least one separate *working piece*" (emphasis added). Differentiating an *overlay* into a *code portion* and a *data portion* is not the same as splitting a segment of *code* into a *controlling piece of code* and a *working piece of code*. Therefore, Appellant respectfully submits that claim 1, and claims 2-12 depending therefrom, are not anticipated by Sherman.

Appellant made the above argument in a Response mailed on February 16, 2005. In response to this argument, the Examiner argued in the Office Action of March 15, 2005, that "Merriam Webster's Collegiate Dictionary, tenth edition define (sic) 'differentiate' as to become distinct and the Microsoft Press Computer Dictionary Third Edition defines "overlay" as a section of a program to reside on a storage device. As it is clear from the above definitions differentiating the overlays into a code and data portions is the same thing as splitting a segment into a controlling and working codes."[4] Appellant has no quarrel with the Examiner's definition of the word "differentiate." But Appellant submits that Sherman does not teach splitting, or differentiating, a segment of code into a *controlling piece of code* and a *working piece of code*, as claimed in claim 1. Rather, Sherman teaches "differentiating the overlays into a *code portion* and into a *data portion*"[5] (emphasis added). This is a significant difference. Furthermore, Sherman does not teach "locating certain *controlling pieces of the program code* in the storage area, and transferring only certain *working pieces of the program code* in the first memory area," as is called for in claim 1 (emphasis added). For at least the foregoing reasons, Appellant submits that claim 1, and claims 2-12 depending therefrom, are not anticipated by Sherman.

For the record, Appellant would also point out that the Examiner's recitation of the definition of "overlay" from the Microsoft Press Computer Dictionary is truncated. The full definition is, "A section of a program designed to reside on a designated storage device, such as a disk, and to be loaded into memory when needed, usually overwriting one or more overlays already in memory."[6]

[3] Sherman patent (US 5,175,830), column 1, lines 65-66.

[4] Office Action dated March 15, 2005, page 2.

[5] Sherman patent, column 1, lines 65-66.

[6] Microsoft Press Computer Dictionary, 3rd Edition,

The Examiner also rejected claims 13-24 as anticipated by Sherman for the same reasons used to reject claims 1-12. Therefore, Appellant submits that claims 13-24 are not anticipated by Sherman for the same reasons set out above with respect to claims 1-12.

B. Claim 25 is not anticipated under 35 U.S.C. § 102(b) by Sherman et al. (US 5,175,830).

Claim 25 is directed to

> 25. A distributed signal processing framework for reducing the memory footprint of a digital signal processing device, the framework comprising:
>
> at least one signal processing algorithm, the algorithm being split into a controlling piece and at least one separate processing piece;
>
> a low-MIPS processor device having a high-memory footprint, whereby the controlling piece is stored and runs on the low-MIPS processor device;
>
> a high-MIPS processor having a low-memory footprint, whereby at least one of the separate processing pieces is stored and runs on the high-MIPS processor device; and
>
> a hardware transfer mechanism for efficiently linking the pieces through the distributed framework..

Regarding claim 25, the Examiner asserted in the Final Office Action, "claims 13-26 encompass the same scope of the invention as those of claims 1-12 in addition of performing the steps method and some units for performing the functions. Therefore, claims 13-26 are rejected for the same reasons as stated above with respect to claims 1-12."[7] Appellant submits that claim 25 does not, in fact, encompass the same scope of the invention as claims 1-12, but rather includes several limitations not contained in claims 1-12.

Appellant submits that claim 25 contains several limitations that are not taught by Sherman. For example, Sherman fails to teach "at least one signal processing algorithm, the algorithm being split into a controlling piece and at least one separate processing piece." Sherman further fails to teach "a low-MIPS processor device having a high-memory footprint, whereby the controlling piece is stored and runs on the low-MIPS

[7] Office Action dated March 15, 2005, page 5.

processor device." Sherman also fails to teach "a high-MIPS processor having a low-memory footprint, whereby at least one of the separate processing pieces is stored and runs on the high-MIPS processor device." For at least these reasons, Appellant submits that claim 25 is not anticipated by Sherman.

II. Conclusion

For at least the foregoing reasons, Appellant submits that claims 1-25 are not anticipated by Sherman. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge $1,520 (to cover the Brief on Appeal Fee of $500 and the Extension of Time Fee of $1,020) and any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: January 17, 2006

Respectfully submitted,

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APPENDIX

(37 C.F.R. § 1.192(c)(9))

The following claims are involved in this appeal:

1. An apparatus for reducing the memory footprint of a first processor device, the apparatus comprising:

a segment of program code which is split into portions including at least one controlling piece and at least one separate working piece;

a storage area for storing certain pieces of the program code;

a first memory area associated with the first processor device for receiving certain portions of the program code; and

a hardware transfer mechanism for efficiently linking the storage area with the first memory area,

wherein the memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and transferring only certain working pieces of the program code in the first memory area.

2. The apparatus of Claim 1, wherein the storage area includes a second memory area associated with second processor device.

3. The apparatus of Claim 2, wherein the first processor device includes a high-MIPS processor device having higher-cost memory.

4. The apparatus of Claim 3, wherein the second processor device include a low-MIPS processor device having lower-cost memory.

5. The apparatus of Claim 3, wherein the high-MIPS processor device includes a digital signal processor (DSP) device.

6. The apparatus of Claim 4, wherein the low-MIPS processor device includes a general microcontroller unit (MCU) device.

7. The apparatus of Claim 2, wherein the working piece is further split into code phases and associated data blocks, which are arranged into code and data segments.

8. The apparatus of Claim 7, wherein a store exists in the second memory area for the segments.

9. The apparatus of Claim 8, wherein further included is a segment manager which copies the segments between the store and the first memory area on an as-needed basis.

10. The apparatus of Claim 9, wherein the segment manager utilizes hardware acceleration to achieve efficient transfers.

11. The apparatus of Claim 9, wherein the segment manager is used to schedule segment management from the first processor.

12. The apparatus of Claim 9, wherein the segment manager is used to schedule segment management from the second processor.

13. An method for reducing the memory footprint of a first processor device, the method comprising the steps of:

splitting a segment of program code into portions including at least one controlling piece and at least one separate working piece;

storing certain portions of the program code in a storage area;

receiving certain portions of the program code in a first memory area associated with the first processor device; and

linking the storage area with the first memory area using an efficient hardware transfer mechanism,

wherein the memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and only certain working pieces of the program code in the first memory area.

14. The method of Claim 13, wherein the storage area includes a second memory area associated with second processor device.

15. The method of Claim 14, wherein the first processor device includes a high-MIPS processor device having higher-cost memory.

16. The method of Claim 15, wherein the second processor device include a low-MIPS processor device having lower-cost memory.

17. The method of Claim 15, wherein the high-MIPS processor device includes a digital signal processor (DSP) device.

18. The method of Claim 16, wherein the low-MIPS processor device includes a general microcontroller unit (MCU) device.

19. The method of Claim 14, wherein the steps further include: splitting the working piece into code phases and associated data blocks, and arranging them into code and data segments.

20. The method of Claim 19, wherein the steps further include creating a store in the second memory area for the segments.

21. The method of Claim 19, wherein the steps further include utilizing a segment manager to copy the segments between the store and the first memory area on an as-needed basis.

22. The method of Claim 21, wherein the segment manager further includes the step of utilizing hardware acceleration to achieve efficient transfers.

23. The method of Claim 21, wherein the steps further include scheduling the segment management, using the segment manager, from the first processor.

24. The method of Claim 21, wherein the steps further include scheduling the segment management, using the segment manager, from the second processor.

25. A distributed signal processing framework for reducing the memory footprint of a digital signal processing device, the framework comprising:

at least one signal processing algorithm, the algorithm being split into a controlling piece and at least one separate processing piece;

a low-MIPS processor device having a high-memory footprint, whereby the controlling piece is stored and runs on the low-MIPS processor device;

a high-MIPS processor having a low-memory footprint, whereby at least one of the separate processing pieces is stored and runs on the high-MIPS processor device; and

a hardware transfer mechanism for efficiently linking the pieces through the distributed framework.